NEC

MOS FIELD EFFECT TRANSISTOR
2SK3060

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK3060 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

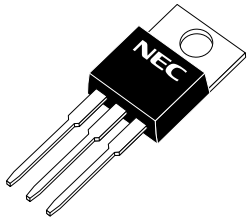
- Low on-state resistance
  $R_{DS(on)1}$ = 13 mΩ MAX. (V_{GS} = 10 V, I_D = 35 A)
  $R_{DS(on)2}$ = 20 mΩ MAX. (V_{GS} = 4.0 V, I_D = 35 A)
- Low C_{iss}: C_{iss} = 2400 pF TYP.
- Built-in gate protection diode

ORDERING INFORMATION

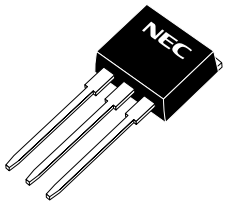
PART NUMBER	PACKAGE
2SK3060	TO-220AB
2SK3060-S	TO-262
2SK3060-ZJ	TO-263
★ 2SK3060-Z	TO-220SMD[Note]

Note This package is produced only in Japan.

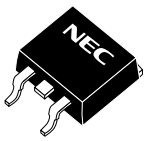
(TO-220AB)



(TO-262)



(TO-263, TO-220SMD)



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	60	V
Gate to Source Voltage (V_{DS} = 0 V)	$V_{GSS(AC)}$	±20	V
Gate to Source Voltage (V_{DS} = 0 V)	$V_{GSS(DC)}$	+20, –10	V
Drain Current (DC)	$I_{D(DC)}$	±70	A
Drain Current (Pulse) [Note1]	$I_{D(pulse)}$	±210	A
Total Power Dissipation (T_C = 25°C)	P_T	70	W
Total Power Dissipation (T_A = 25°C)	P_T	1.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current [Note2]	I_{AS}	35	A
Single Avalanche Energy [Note2]	E_{AS}	122.5	mJ

Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1%

2. Starting T_{ch} = 25°C, R_G = 25 Ω, V_{GS} = 20 V → 0 V

THERMAL RESISTANCE

Channel to Case	$R_{th(ch-C)}$	1.79	°C/W
Channel to Ambient	$R_{th(ch-A)}$	83.3	°C/W

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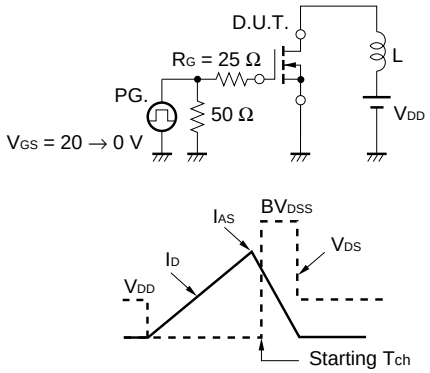
The mark ★ shows major revised points.

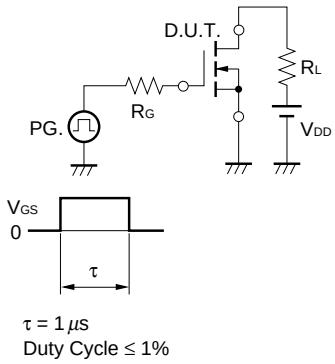
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 35 A		11	13	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.0 V, I_D = 35 A		16	20	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.0	1.5	2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 35 A	15	50		S
Drain Leakage Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 10 V V_{GS} = 0 V f = 1 MHz		2400		pF
Output Capacitance	C_{oss}			700		pF
Reverse Transfer Capacitance	C_{rss}			280		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 35 A $V_{GS(on)}$ = 10 V V_{DD} = 30 V R_G = 10 Ω		30		ns
Rise Time	t_r			600		ns
Turn-off Delay Time	$t_{d(off)}$			140		ns
Fall Time	t_f			450		ns
Total Gate Charge	Q_G	I_D = 70 A V_{DD} = 48 V V_{GS} = 10 V		50		nC
Gate to Source Charge	Q_{GS}			7.5		nC
Gate to Drain Charge	Q_{GD}			18		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 70 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 70 A, V_{GS} = 0 V di/dt = 100 A/μs		55		ns
Reverse Recovery Charge	Q_{rr}			75		nC

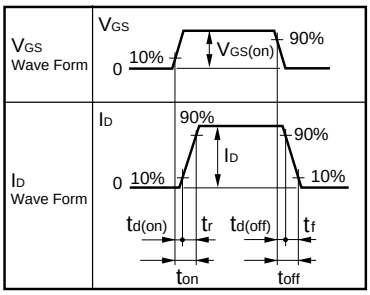
TEST CIRCUIT 1 AVALANCHE CAPABILITY



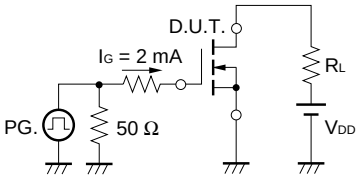
TEST CIRCUIT 2 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1%

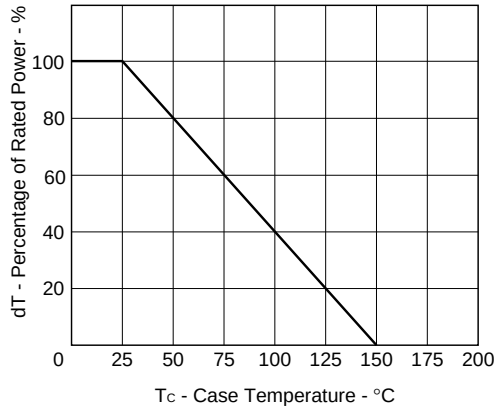


TEST CIRCUIT 3 GATE CHARGE

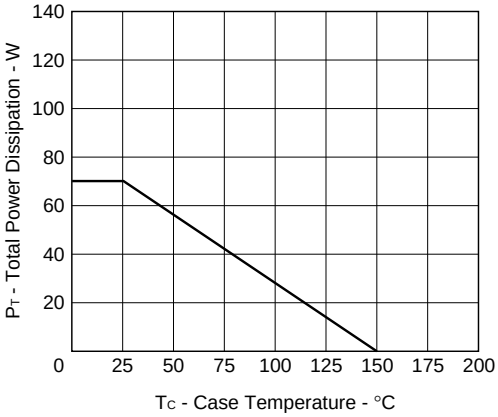


TYPICAL CHARACTERISTICS (T_A = 25°C)

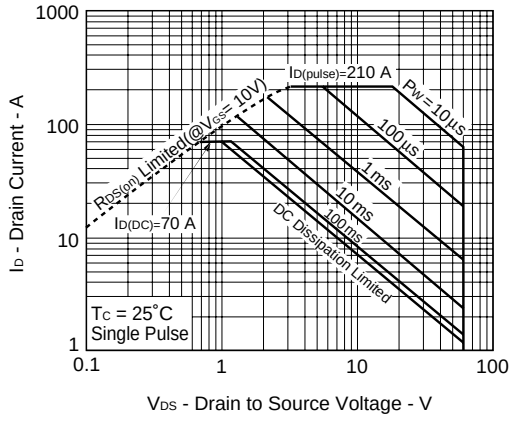
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



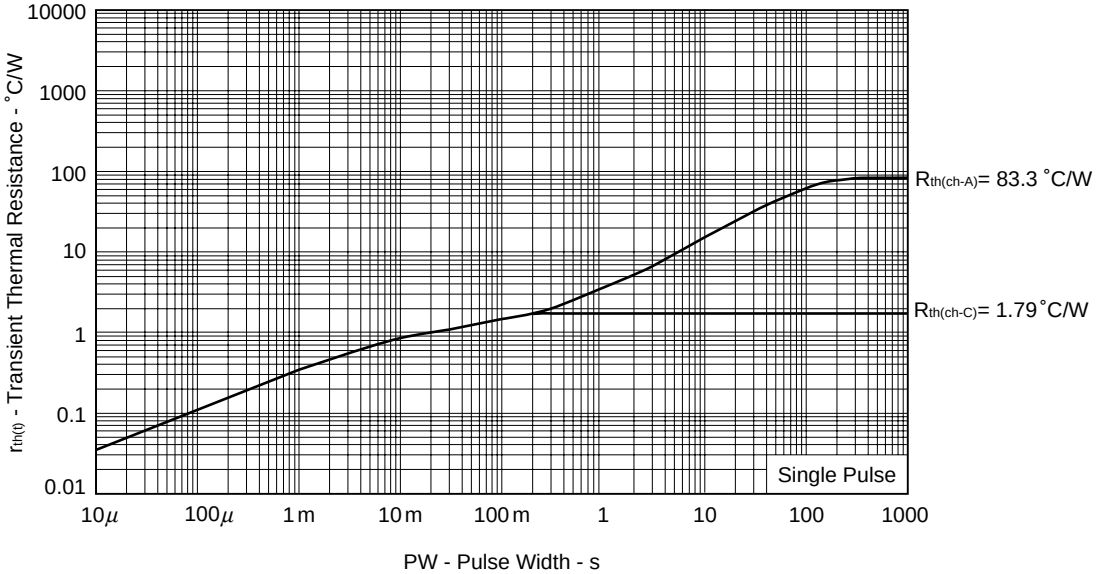
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



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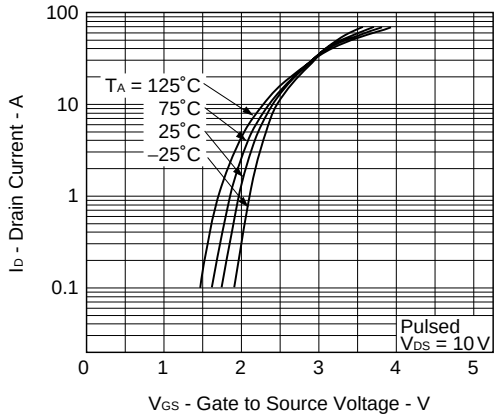
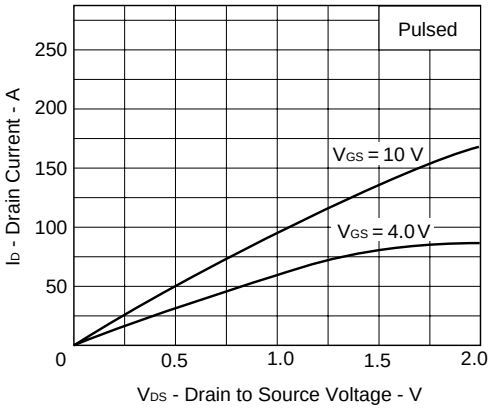
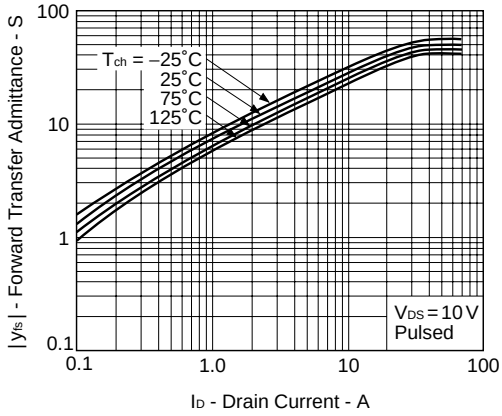
FORWARD TRANSFER CHARACTERISTICS



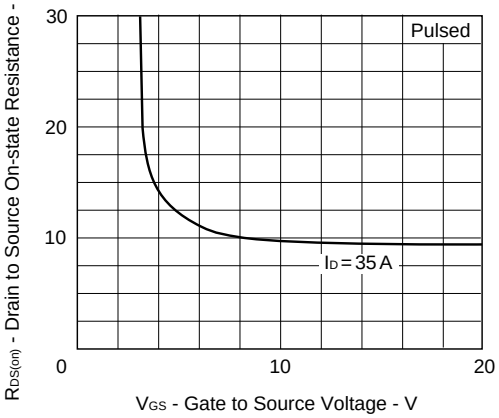
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



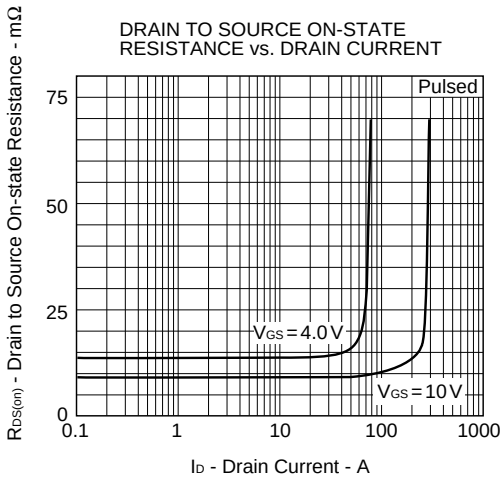
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



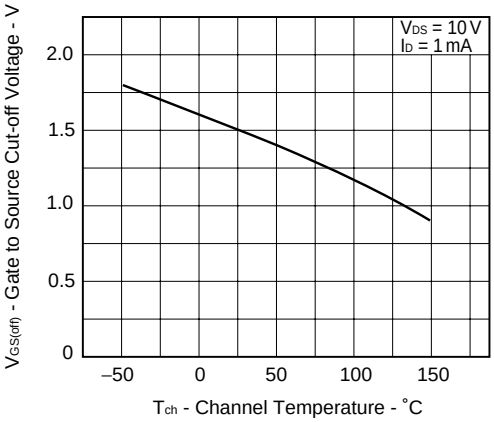
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



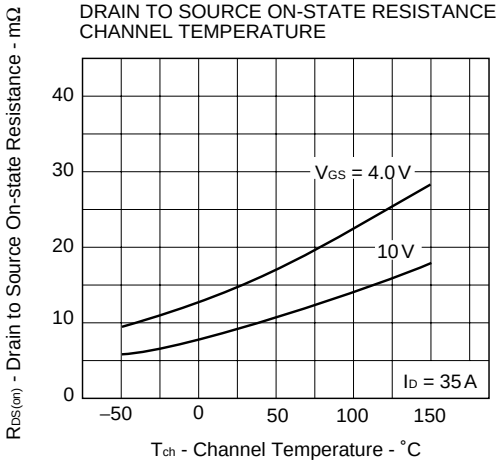
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



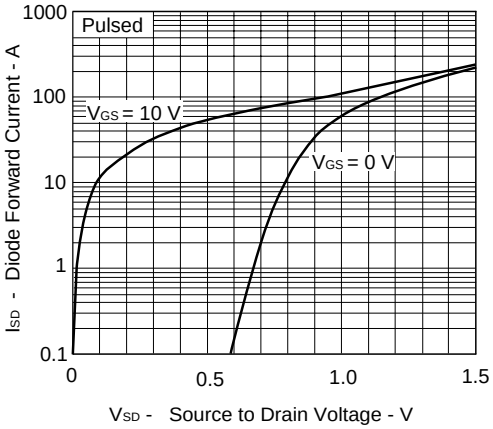
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



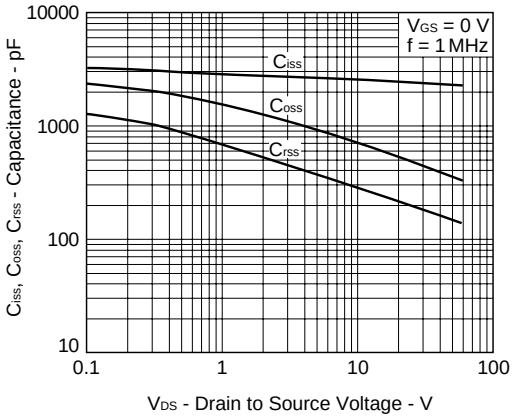
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



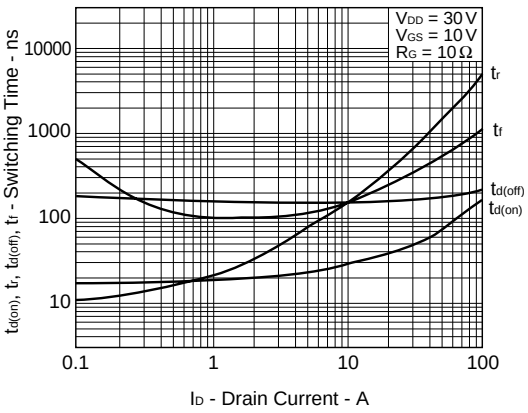
★ SOURCE TO DRAIN DIODE FORWARD VOLTAGE



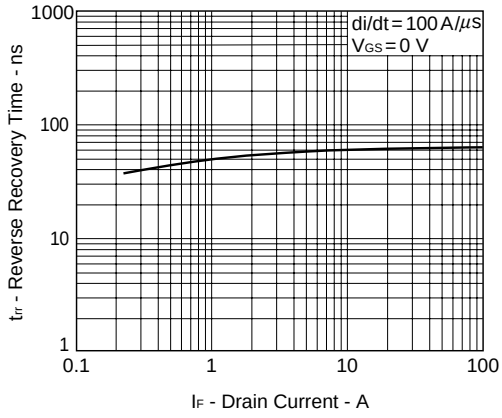
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



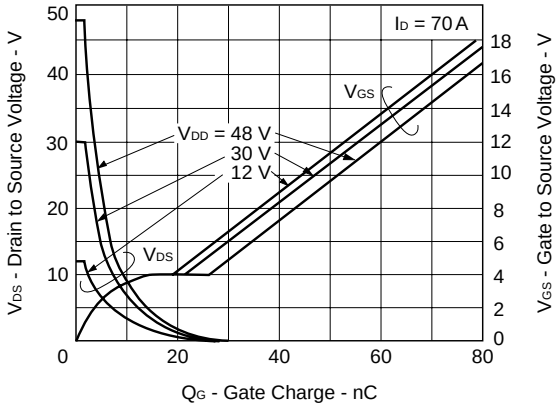
SWITCHING CHARACTERISTICS



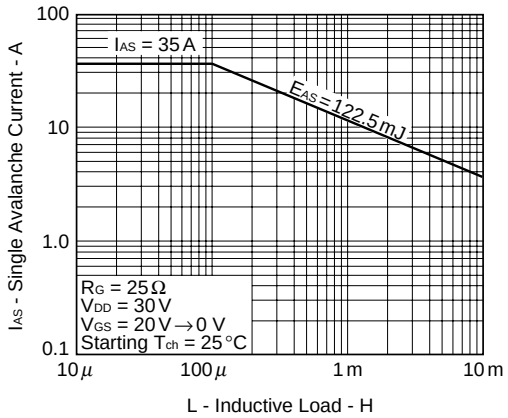
REVERSE RECOVERY TIME vs. DRAIN CURRENT



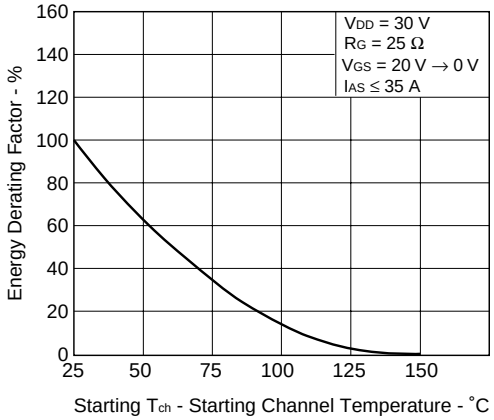
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

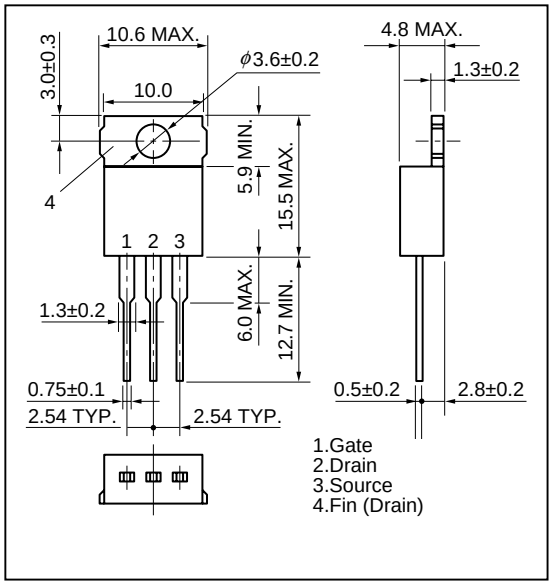


SINGLE AVALANCHE ENERGY
DERATING FACTOR

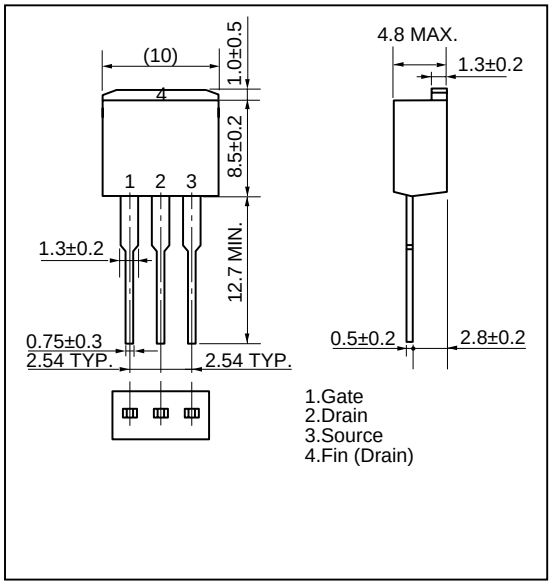


PACKAGE DRAWINGS (Unit : mm)

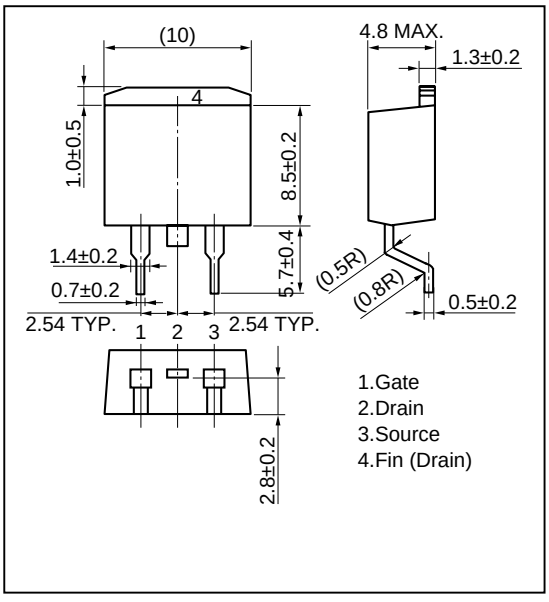
1)TO-220AB (MP-25)



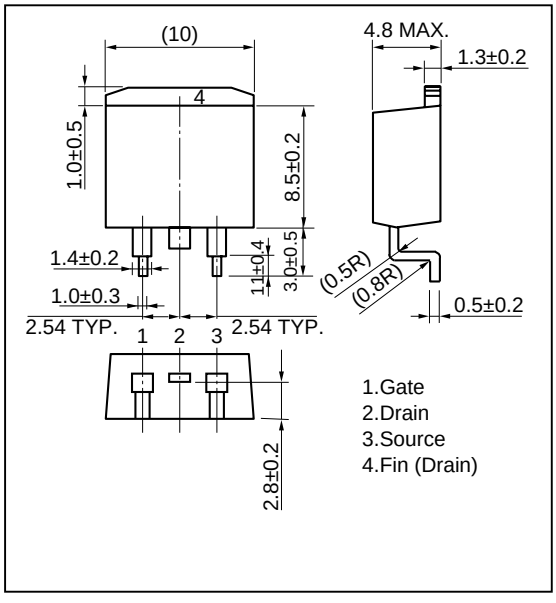
2)TO-262 (MP-25 Fin Cut)



3)TO-263 (MP-25ZJ)

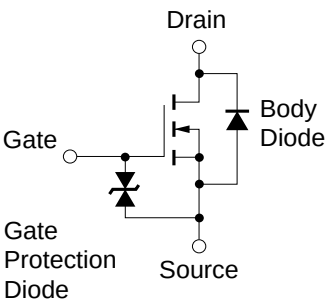


★ 4)TO-220SMD (MP-25Z) Note



Note This package is produced only in Japan.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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